Monolithic 3D integration using 2D-assisted epitaxy and growth

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The continuous scaling of current electronic system faces fundamental physical and thermal limits, necessitating a paradigm shift toward three-dimensional (3D) integration. While through-silicon-via (TSV) technologies enable partial 3D stacking, they suffer from parasitic losses and limited density. Monolithic 3D (M3D) integration in this regard offers a transformative alternative by vertically stacking active device layers with direct inter-tier interconnects. However, realizing single-crystalline channels in upper tiers at low thermal budgets remains a major bottleneck. Two-dimensional (2D) semiconductors—atomically thin materials that preserve high carrier mobility even at sub-nanometer thickness—provide a unique opportunity to overcome this challenge. Their van der Waals interfaces allow layer-by-layer growth or transfer onto amorphous or polycrystalline surfaces, enabling seamless M3D fabrication compatible with back-end-of-line (BEOL) processes. In this talk, recent approaches based on 2D-assisted growth and device-level demonstrations will be addressed. This emerging direction of 2D-based M3D integration paves the way for energy-efficient, high-density, and functionally diverse electronics beyond the limits of conventional silicon scaling with high density of chips.